

Docket No. AUS920030554US1

CLAIMS:

What is claimed is:

1. A method, in a multiprocessor data processing system, for identifying false sharing of a cache line, comprising:

associating a performance indicator with at least one portion of a cache line in a cache;

providing a plurality of processor access flag bits for the at least one portion of the cache line in the cache, wherein there is at least one processor access flag bit for each processor of a plurality of processors in the multiprocessor data processing system; and

responsive to an access operation to the at least one portion of the cache line, setting a processor access flag bit corresponding to a processor from which the access operation was received.

2. The method of claim 1, further comprising:

in response to a reload of the cache line due to an access operation from a current processor of the plurality of processors targeting a current portion of the cache line, reading values of the processor access flag bits for each portion of the cache line; and

determining if the reload operation is due to false sharing of the cache line based on the values of the processor access flag bits for each portion of the cache line.

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3. The method of claim 2, wherein determining if the reload operation is due to false sharing of the cache line includes:

comparing a first value of a first processor access flag bit associated with the current processor and the current portion of the cache line, to values of second processor access flag bits associated with other processors of the plurality of processors and the current portion of the cache line; and

determining that true cache line sharing is present if a first predetermined relationship between the value of the first processor access flag bit and the values of the second processor access flag bits is present.

4. The method of claim 3, further comprising:

comparing the first value of the first processor access flag bit with values of third processor access flag bits associated with other processors and another portion of the cache line; and

determining that false cache line sharing is present if a second predetermined relationship between the value of the first processor access flag bit, the values of the second processor access flag bits, and the values of the third processor access flag bits is present.

5. The method of claim 3, wherein the first predetermined relationship is that at least one of the second processor access flag bits is set and the first processor access flag bit is set.

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6. The method of claim 4, wherein the second predetermined relationship is that at least one of the third processor access flag bits is set, a corresponding one of the second processor access flag bits is not set, and the first processor access flag bit is set.

7. The method of claim 2, further comprising:
outputting an indication that there is false cache line sharing if the reload operation is determined to be due to false sharing of the cache line.

8. A computer program product in a computer readable medium for identifying false sharing of a cache line, comprising:

first instructions for associating a performance indicator with at least one portion of a cache line in a cache;

second instructions for providing a plurality of processor access flag bits for the at least one portion of the cache line in the cache, wherein there is at least one processor access flag bit for each processor of a plurality of processors in a multiprocessor data processing system; and

third instructions for responsive to an access operation to the at least one portion of the cache line, setting a processor access flag bit corresponding to a processor from which the access operation was received.

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9. The computer program product of claim 8, further comprising:

fourth instructions for reading values of the processor access flag bits for each portion of the cache line, in response to a reload of the cache line due to an access operation from a current processor of the plurality of processors targeting a current portion of the cache line; and

fifth instructions for determining if the reload operation is due to false sharing of the cache line based on the values of the processor access flag bits for each portion of the cache line.

10. The computer program product of claim 9, wherein the fifth instructions for determining if the reload operation is due to false sharing of the cache line include:

instructions for comparing a first value of a first processor access flag bit associated with the current processor and the current portion to values of second processor access flag bits associated with other processors of the plurality of processors and the current portion; and

instructions for determining that true cache line sharing is present if a first predetermined relationship between the value of the first processor access flag bit and the values of the second processor access flag bits is present.

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11. The computer program product of claim 10, further comprising:

instructions for comparing the first value of the first processor access flag bit with values of third processor access flag bits associated with other processors and another portion of the cache line; and

instructions for determining that false cache line sharing is present if a second predetermined relationship between the value of the first processor access flag bit, the values of the second processor access flag bits, and the values of the third processor access flag bits is present.

12. The computer program product of claim 10, wherein the first predetermined relationship is that at least one of the second processor access flag bits is set and the first processor access flag bit is set.

13. The computer program product of claim 11, wherein the second predetermined relationship is that at least one of the third processor access flag bits is set, a corresponding one of the second processor access flag bits is not set, and the first processor access flag bit is set.

14. The computer program product of claim 9, further comprising:

sixth instructions for outputting an indication that there is false cache line sharing if the reload operation

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is determined to be due to false sharing of the cache line.

15. An apparatus, in a multiprocessor data processing system, for identifying false sharing of a cache line, comprising:

means for associating a performance indicator with at least one portion of a cache line in a cache;

means for providing a plurality of processor access flag bits for the at least one portion of the cache line in the cache, wherein there is at least one processor access flag bit for each processor of a plurality of processors in the multiprocessor data processing system; and

means for responsive to an access operation to the at least one portion of the cache line, setting a processor access flag bit corresponding to a processor from which the access operation was received.

16. The apparatus of claim 15, further comprising:

means for reading values of the processor access flag bits for each portion of the cache line, in response to a reload of the cache line due to an access operation from a current processor of the plurality of processors targeting a current portion of the cache line; and

means for determining if the reload operation is due to false sharing of the cache line based on the values of the processor access flag bits for each portion of the cache line.

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17. The apparatus of claim 16, wherein the means for determining if the reload operation is due to false sharing of the cache line includes:

means for comparing a first value of a first processor access flag bit associated with the current processor and the current portion to values of second processor access flag bits associated with other processors of the plurality of processors and the current portion; and

means for determining that true cache line sharing is present if a first predetermined relationship between the value of the first processor access flag bit and the values of the second processor access flag bits is present.

18. The apparatus of claim 17, further comprising:

means for comparing the first value of the first processor access flag bit with values of third processor access flag bits associated with other processors and another portion of the cache line; and

means for determining that false cache line sharing is present if a second predetermined relationship between the value of the first processor access flag bit, the values of the second processor access flag bits, and the values of the third processor access flag bits is present.

19. The apparatus of claim 17, wherein the first predetermined relationship is that at least one of the

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second processor access flag bits is set and the first processor access flag bit is set.

20. The apparatus of claim 18, wherein the second predetermined relationship is that at least one of the third processor access flag bits is set, a corresponding one of the second processor access flag bits is not set, and the first processor access flag bit is set.

21. The apparatus of claim 16, further comprising:

means for outputting an indication that there is false cache line sharing if the reload operation is determined to be due to false sharing of the cache line.